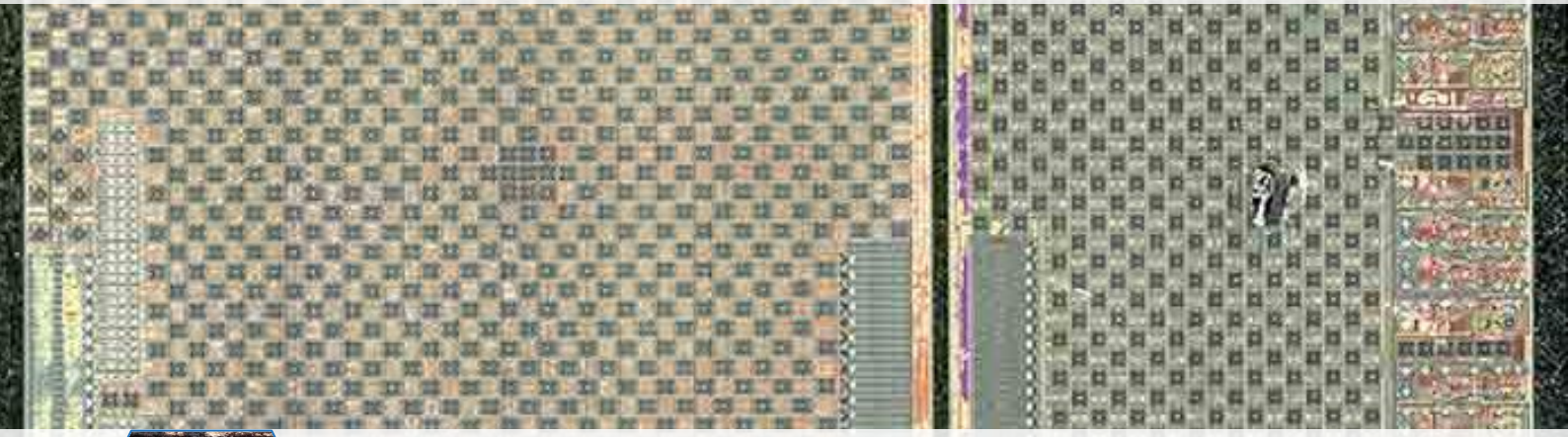
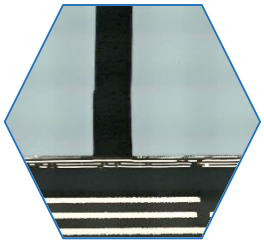
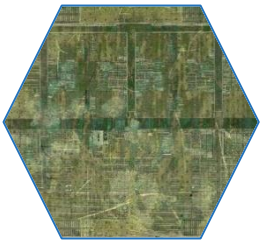


HiSilicon Hi1382 Coherent Processor with ASE's FOCoS

Extensive analysis of Fan-Out Chip on Substrate technology from ASE used in Baseband Unit Processor from Huawei.





Title: HiSilicon Hi1382 Coherent Processor with ASE's FOCoS

Pages: 152

Date: June 2021

Format: PDF & Excel file

Reference: SPR21622

In Fan-Out (FO) packaging technology, a battle is raging between Outsourced Semiconductor Assembly and Test (OSAT) companies and foundries. OSAT companies are mainly supplying small components with FO technology. In high-end applications, the penetration of the technology started with TSMC in consumer applications in partnership with Apple. In parallel, several players like ASE are working on industrial applications where the use of FO is expected to increase. In High Performance Computing the technology is trying to compete with interposer-based assembly. Today, Original Equipment Manufacturers prefer the use of Chip on Wafer On Substrate technologies for Graphic Processing Unit and Dynamic Random Access Memory assembly. But for applications like interfacing and switching, FO technology brought shorter interconnection providing high speed communication.

Nephos chose TSMC's integrated Fan-Out on Substrate (inFO_oS) technology for its high-speed switching device. However, Huawei, via HiSilicon, chose ASE's Fan-Out Chip on Substrate (FOCoS) for its coherent processor, the Hi1382.

The Hi1382 is a processor included in the Baseband Unit (BBU) BBU5900 for Huawei in two different layers. One is in the universal baseband processor unit and one is in the Universal Main Processing and Transmission Unit. On both cards, the coherent processor manages the interface between the optical fiber module and the network processors. To ensure high speed interconnecting between the entities, ASE's fan-out packaging technology has been selected and implemented. The technology allows heterogenous structure in the integrated circuit design by interfacing a System-on-Chip die based on 16-nm technology node with a transceiver die based on 28-nm technology node.

This report includes a full investigation of the component, featuring a detailed study of the System-in-Package, including die analyses, processes, and package cross-sections. It contains a complete cost analysis and a selling price estimation of the component.

COMPLETE TEARDOWN WITH

- Detailed photos
- Precise measurements
- Materials analysis
- Manufacturing process flow
- Supply chain evaluation
- Manufacturing cost analysis

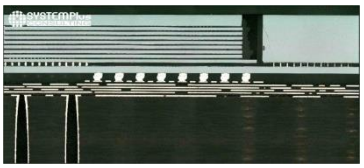
TABLE OF CONTENTS

AUTHORS

Stéphane Elisabeth, PhD *is Expert Cost Analyst in RF, Sensors and Advanced Packaging. He has a deep knowledge of materials characterizations and electronics systems. He holds an Engineering Degree in Electronics and Numerical Technology, and a PhD in Materials for Microelectronics.*

Peggy Gallois *joined System Plus Consulting's laboratory of micro-electronics team in July 2019. She previously worked in the laboratory of metallographic exper-tise for Dassault Aviation near Paris.*

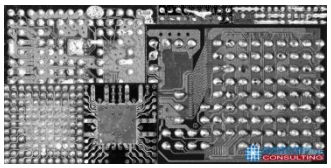
RELATED ANALYSES



NVIDIA A100 Ampere GPU

NVIDIA's new generation Graphics Processing Unit (GPU) with TSMC CoWoS, 40GB Samsung HBM2, 2.5D and 3D packaging.

February 2021



Fan-Out Packaging Processes Comparison 2020

In-depth technical and cost overview of key Fan-Out process technologies form Infineon, nepes, TSMC, SEMCO and ASE.

February 2020

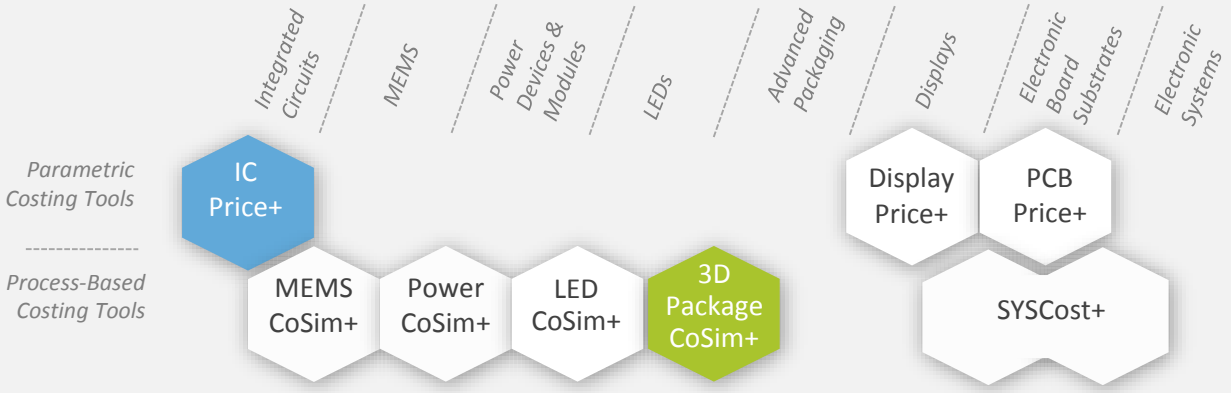
Fan-Out WLP and PLP Applications and Technologies 2021

TSMC's Fan-Out success with Apple and high-performance computing are pushing Intel, Samsung, ASE, and all other competitor s to find new innovative solutions.

June 2021

SYSTEMPlus CONSULTING

COSTING TOOLS



Our analysis is performed with our costing tools IC Price+ and 3D Packaging CoSim+.

System Plus Consulting offers powerful costing tools to evaluate the production cost and selling price from single chip to complex structures.

IC Price+
The tool performs the necessary cost simulation of any Integrated Circuit: ASICs, microcontrollers, memories, DSP, smartpower…

3D Packaging CoSim+
Cost simulation tool to evaluate the cost of any Packaging process: Wafer-level packaging, TSV, 3D integration…

WHAT IS A REVERSE COSTING®?

Reverse Costing® is the process of disassembling a device (or a system) in order to identify its technology and calculate its manufacturing cost, using in-house models and tools.

CONTACTS

Headquarters
22, bd Benoni Goullin
Nantes Biotech
44200 Nantes
France
+33 2 40 18 09 16
sales@systemplus.fr

Europe Sales Office
Lizzie LEVENEZ
Frankfurt am Main
Germany
+49 151 23 54 41 82
llevenez@systemplus.fr

America Sales Office
Steven LAFERRIERE
Western USA & Canada
+1 310-600-8267
laferriere@yole.fr

Chris YOUMAN
Eastern USA & Canada
+1 919-607-9839
chris.youman@yole.fr

Asia Sales Office
Takashi ONOZAWA
Japan & Rest of Asia
+81 80 4371 4887
onozawa@yole.fr

Mavis WANG
Greater China
TW +886 979 336 809
CN +8613661566824
wang@yole.fr

Peter OK
Korea
+82 10 4089 0233
peter.ok@yole.fr

ABOUT SYSTEM PLUS CONSULTING

System Plus Consulting is specialized in the cost analysis of electronics from semiconductor devices to electronic systems.
A complete range of services and costing tools to provide in-depth production cost studies and to estimate the objective selling price of a product is available.

Our services:

- **STRUCTURE & PROCESS ANALYSES**
- **TEARDOWNS**
- **CUSTOM ANALYSES**
- **COSTING SERVICES**
- **COSTING TOOLS**
- **TRAININGS**

www.systemplus.fr
sales@systemplus.fr

SYSTEMPlus CONSULTING